CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (withdrawn): A storage capacitor, comprising:

a lower capacitor electrode;

a storage dielectric; and

an upper capacitor electrode;

at least one of said lower and upper capacitor electrodes being a conductive layer;

a doped layer selected from the group consisting of a SiGe layer, a SiC layer, and a GaAs layer or a doped filling selected from the group consisting of a SiGe filling, a SiC filling, and a GaAs filling disposed between said conductive layer and said storage dielectric; and

wherein a doped SiGe layer is not disposed between said storage dielectric and said upper capacitor electrode.

Claim 2 (withdrawn): The storage capacitor according to claim 1 configured to form a part of a DRAM memory cell.

Claim 3 (withdrawn): The storage capacitor according to claim 1, wherein a dopant for said SiGe layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

Claim 4 (withdrawn): The storage capacitor according to claim 1, wherein a dopant for said SiC layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

Claim 5 (withdrawn): The storage capacitor according to claim 1, wherein said conductive layer is formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN.

Claim 6 (withdrawn): The storage capacitor according to claim 1, wherein said storage dielectric contains a material selected from the group consisting of silicon nitride, silicon dioxide, silicon oxynitride, metal oxide, aluminum oxide, Pr_2O_3, Nd_2O_3, Al_2O_3 with an addition of Hf, Zr, Y or La.

Claim 7 (withdrawn): The storage capacitor according to claim 1, wherein said doped layer has a dopant distribution with a gradient.

Claim 8 (currently amended): A storage capacitor, comprising:

a lower capacitor electrode;

a storage dielectric; and

an upper capacitor electrode;

~~at least one of~~ said lower ~~and upper~~ capacitor ~~electrodes~~ electrode being a conductive layer;

a doped layer selected from the group consisting of a SiGe layer, a SiC layer, and a GaAs layer or a doped filling selected from the group consisting of a SiGe filling, a SiC filling, and a GaAs filling disposed on a side of said conductive layer remote from said storage dielectric; and

wherein a doped SiGe layer is not disposed between said storage dielectric and said upper capacitor electrode.

Claim 9 (original): The storage capacitor according to claim 8 configured to form a part of a DRAM memory cell.

Claim 10 (original): The storage capacitor according to claim 8, wherein a dopant for said SiGe layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

Claim 11 (withdrawn): The storage capacitor according to claim 8, wherein a dopant for said SiC layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

Claim 12 (original): The storage capacitor according to claim 8, wherein said conductive layer is formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN.

Claim 13 (original): The storage capacitor according to claim 8, wherein said storage dielectric contains a material selected from the group consisting of silicon nitride, silicon dioxide, silicon oxynitride, metal oxide, aluminum oxide, Pr_2O_3, Nd_2O_3, Al_2O_3 with an addition of Hf, Zr, Y or La.

Claim 14 (original): The storage capacitor according to claim 8, wherein said doped layer has a dopant distribution with a gradient.

Claim 15 (withdrawn): A storage capacitor, comprising:

a conductive layer forming a lower capacitor electrode;

a storage dielectric;

an upper capacitor electrode; and

a doped Si layer disposed between said conductive layer and said storage dielectric.

Claim 16 (withdrawn): The storage capacitor according to claim 15 configured to form a part of a DRAM memory cell.

Claim 17 (withdrawn): The storage capacitor according to claim 15, wherein a dopant for said Si layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

Claim 18 (withdrawn): The storage capacitor according to claim 15, wherein said conductive layer is formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN.

Claim 19 (withdrawn): The storage capacitor according to claim 15, wherein said storage dielectric contains a material selected from the group consisting of silicon nitride, silicon dioxide, silicon oxynitride, metal oxide, aluminum oxide, Pr_2O_3, Nd_2O_3, Al_2O_3 with an addition of Hf, Zr, Y or La.

Claim 20 (withdrawn): The storage capacitor according to claim 15, wherein said Si layer contains a dopant introduced with a gradient.

Claim 21 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 1 formed as a trench capacitor with an upper capacitor electrode;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said upper capacitor electrode is electrically connected to one of said source and drain electrodes.

Claim 22 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 8 formed as a trench capacitor with an upper capacitor electrode;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said upper capacitor electrode is electrically connected to one of said source and drain electrodes.

Claim 23 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 15 formed as a trench capacitor with an upper capacitor electrode;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said upper capacitor electrode is electrically connected to one of said source and drain electrodes.

Claim 24 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 1 formed as a stacked capacitor and having the lower capacitor electrode applied on a connection structure;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said lower capacitor electrode is electrically conductively connected to one of said source and drain electrodes via said connection structure.

Claim 25 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 8 formed as a stacked capacitor and having the lower capacitor electrode applied on a connection structure;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said lower capacitor electrode is electrically conductively connected to one of said source and drain electrodes via said connection structure.

Claim 26 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 15 formed as a stacked capacitor and having the lower capacitor electrode applied on a connection structure;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said lower capacitor electrode is electrically conductively connected to one of said source and drain electrodes via said connection structure.

Claim 27(withdrawn): A storage capacitor, comprising:

a lower capacitor electrode;

a storage dielectric; and

an upper capacitor electrode;

at least one of said lower and upper capacitor electrodes being a conductive filling;

a doped layer selected from the group consisting of a SiGe layer, a SiC layer, and a GaAs layer disposed between said conductive filling and said storage dielectric; and

wherein a doped SiGe layer is not disposed between said storage dielectric and said upper capacitor electrode.

Claim 28 (withdrawn): The storage capacitor according to claim 27 configured to form a part of a DRAM memory cell.

Claim 29 (withdrawn): The storage capacitor according to claim 27, wherein a dopant for said SiGe layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

Claim 30 (withdrawn): The storage capacitor according to claim 27, wherein a dopant for said SiC layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

Claim 31 (withdrawn): The storage capacitor according to claim 27, wherein said conductive layer is formed of a material selected from the group consisting of metal

silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN.

Claim 32 (withdrawn): The storage capacitor according to claim 27, wherein said storage dielectric contains a material selected from the group consisting of silicon nitride, silicon dioxide, silicon oxynitride, metal oxide, aluminum oxide, Pr_2O_3, Nd_2O_3, Al_2O_3 with an addition of Hf, Zr, Y or La.

Claim 33 (withdrawn): The storage capacitor according to claim 27, wherein said doped layer has a dopant distribution with a gradient.

Claim 34 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 27 formed as a trench capacitor with an upper capacitor electrode;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said upper capacitor electrode is electrically connected to one of said source and drain electrodes.

Claim 35 (withdrawn): A memory cell, comprising:

a storage capacitor according to claim 27 formed as a stacked capacitor and having the lower capacitor electrode applied on a connection structure;

a selection transistor having a source electrode, a drain electrode, a gate electrode, and a conductive channel; and

wherein said lower capacitor electrode is electrically conductively connected to one of said source and drain electrodes via said connection structure.

Claim 36 (new): A storage capacitor, comprising:

a substrate having a trench formed therein, said trench having a bottom, an upper portion and a lower portion with sidewalls;

a collar disposed in said upper portion of said trench;

a lower capacitor electrode;

a storage dielectric covering said lower portion of said trench and said collar;

an upper capacitor electrode being a conductive layer disposed at said sidewalls of said lower portion of said trench and at said bottom of said trench;

a doped layer selected from the group consisting of a SiGe layer, a SiC layer, and a GaAs layer or a doped filling selected from the group consisting of a SiGe filling, a SiC filling, and a GaAs filling disposed on a side of said conductive layer remote from said storage dielectric, said doped layer or said filling covering said upper capacitor electrode and said storage dielectric at said upper portion of said trench; and

said storage dielectric and said upper capacitor electrode having no doped SiGe layer disposed therebetween.

Claim 37 (new): The storage capacitor according to claim 36, configured to form a part of a DRAM memory cell.

Claim 38 (new): The storage capacitor according to claim 36, wherein a dopant for said SiGe layer is selected from the group consisting of Al, Ga, In, Tl, B, As, Sb, and P.

Claim 39 (new): The storage capacitor according to claim 36, wherein said conductive layer is formed of a material selected from the group consisting of metal silicide, metal nitride, metal carbide, WN, WSiN, WC, TiN, TaN, and TaSiN.

Claim 40 (new): The storage capacitor according to claim 36, wherein said storage dielectric contains a material selected from the group consisting of silicon nitride, silicon dioxide, silicon oxynitride, metal oxide, aluminum oxide, Pr_2O_3, Nd_2O_3, Al_2O_3 with an addition of Hf, Zr, Y or La.

Claim 41 (new): The storage capacitor according to claim 36, wherein said doped layer has a dopant distribution with a gradient.